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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,248	03/31/2004	William Hugh Cochran	ROC920030326US1	8154

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 08/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,248	COCHRAN ET AL.	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8,10-14 and 16-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8,10-14 and 16-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a FINAL Office Action in response to Amendment filed 7/13/2006.

Claims 1-20 were previously examined. Claims 3, 9, 15 and 20 have been cancelled. Claims 1, 17 and 18 have been amended. Claims 1, 2, 4-8,10-14 and 16-19 are pending in the instant Application.

Objection to the abstract of the disclosure is hereby withdrawn, in view of the amendment to the Abstract as required by the prior Office Action.

Response to Arguments

Applicant's arguments filed 7/13/2006, with respect to Claims 1, 2, 4-8 and 16-19, have been fully considered but they are not persuasive.

In reference to independent claims 1 and 17 as currently amended, Applicant argues, page 10, that Pochmuller (US 6,295,237) fails to suggest or disclose an MBIST engine, including MBIST control circuitry and MBIST registers, using the at least one monitor element with the MBIST engine to identify an approaching failing situation for enabling appropriate preventative action, and providing latch circuitry coupled to the MBIST engine for latching monitor bits, the latch circuitry is used to communicate with the MBIST engine.

In response to Applicant's argument with respect to claimed feature of "MBIST control circuitry and MBIST registers", Pochmuller discloses, Figure 6, a built-in-self-test (BIST) computing unit 14 including a control circuitry such as a counter unit 15 for

counting the hit values up to an upper limit and then evaluating the results of the tests, which are being stored in the registers 12.

In response to Applicant's argument with respect to claimed feature of "using the at least one monitor element with the MBIST engine to identify an approaching failing situation for enabling appropriate preventative action", the expression "approaching failing situation" renders the claims indefinite, because the term "approaching" does not positively define the occurrence of a failure or degradation in the integrated circuit under test. In this case, the term "approaching" does not imply that a failure has already occurred in the integrated circuit, since the ordinary meaning implies to draw closer, to come very near to, or to make advances to especially in order to create a desired result. Therefore, it is not clear how one of ordinary skill in the art could use a monitor element to identify a failure that has not yet occurred. Furthermore, the specification does not adequately describe how a monitor element can identify an approaching failing situation, or at least provide a standard for ascertaining the requisite degree, so that one of ordinary skill in the art would be able to make or use the invention.

Nevertheless, in view of the rejection under 35 U.S.C. 112, second paragraph, with respect to claimed feature of "approaching failing situation" as indicated in the Office Action, the Examiner interprets the above limitation to correspond to the test feature, as disclosed by Pochmuller, of individual memory cell arrays being checked by driving their word lines and bit lines in order to determine defective memory cells, where the results finally being stored in the registers 12. A built-in-self-test (BIST) computing unit 14 with a counter unit 15 for counting the hit values up to an upper limit then

evaluates the results of the tests. The results finally being stored in the registers 12, after the conclusion of the tests and determines those redundant memory cells, bit lines and word lines which, as the spare memory cells, spare bit lines and spare word lines from the memory cell array 10, are intended to replace the defective memory cells, bit lines and word lines in the memory cell arrays 1, 2, . . . , n, as described with respect to Figure 6.

Further Applicant argues that Pochmuller does not show, nor remotely suggest that using the MBIST engine for controlling operation of the at least one monitor element for communicating monitor bits, and for identifying the degradation of signal, timing and voltage margins utilizing said at least one monitor element.

In response to Applicant's argument with respect to claimed feature of "using the MBIST engine for controlling operation of the at least one monitor element for communicating monitor bits", as indicated previously, Pochmuller discloses, Figure 6, a built-in-self-test (BIST) computing unit 14 with a counter unit 15 for counting the hit values up to an upper limit, thus controlling the operation, by evaluating the results of the tests which are then being stored in the registers 12. In reference to the broadly recited limitation of "identifying the degradation of signal, timing and voltage margins", clearly Pochmuller discloses the test feature of determining defective memory cells of individual memory cell arrays by driving their word lines and bit lines, where the test results are stored in the registers 12. Clearly, timing and voltage degradation of a signal is associated with defective memory cells, which could be observed during read out of the test results stored in the registers 12. According to MPEP 2111, CLAIMS MUST BE

GIVEN THEIR BROADEST REASONABLE INTERPRETATION. During patent examination, the pending claims must be given their broadest reasonable interpretation consistent with the specification. In re Hyatt, 211 F.3d 1367, 1372, 54 USPQ2d 1664, 1667 (Fed. Cir. 2000). Applicant always has the opportunity to amend the claims during prosecution, and broad interpretation by the examiner reduces the possibility that the claim, once issued, will be interpreted more broadly than is justified. In re Prater, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-51 (CCPA 1969). In this case, claims 1 and 17 recite the broad limitation of "identifying the degradation of signal, timing and voltage margins", which can be associated with any memory cell failure causing timing and voltage degradation of a signal.

Claims 1, 2, 4-8,10-14 and 16-19 are rejected under 35 U.S.C. 112, second paragraph; Claims 1, 2, 4-8,10-14 and 16-19 are still rejected under 35 U.S.C. 102(b) as being anticipated by Pochmuller (US 6,295,237) as set forth in the present Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims1, 2, 4-8,10-14 and 16-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 17 recite the limitation "approaching failing situation", which renders the claims indefinite, because the term "approaching" does not positively define the occurrence of a failure or degradation in the integrated circuit under test. In this case, the term "approaching" does not imply that a failure has already occurred in the integrated circuit, since the ordinary meaning implies to draw closer, to come very near to, or to make advances to especially in order to create a desired result. Therefore, it is not clear how one of ordinary skill in the art could use a monitor element to identify a failure that has not yet occurred. Furthermore, the specification does not adequately describe how a monitor element can identify an approaching failing situation, or at least provide a standard for ascertaining the requisite degree, so that one of ordinary skill in the art would be able to make or use the invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-8,10-14 and 16-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Pochmuller (US 6,295,237) issued: September 25, 2001.

Regarding independent Claims 1, 17, Pochmuller discloses a method and apparatus for a semiconductor memory configuration, such as a DRAM, in which

redundant memory cells, bit lines and word lines are determined for failed memory cells, failed word lines and failed bit lines by a built-in-self-test (BIST) computing unit (see, Abstract), the method and apparatus comprising:

A semiconductor chip, word lines (WL), bit lines (BL) and a memory cell array disposed on the semiconductor chip and addressed via the word lines and the bit lines, the memory cell array having a multiplicity of memory cells (MC) Figure 1;

Redundant memory cells disposed on the semiconductor chip and addressed by the word lines and the bit lines, the redundant memory cells in an event of failed memory cells of the memory cell array replace the failed memory cells as spare memory cells, (See Summary of the Invention); and

A built-in-self-test (BIST) computing unit disposed on the semiconductor chip and connected to the memory cell array and the redundant memory cells, the BIST computing unit assigning the spare memory cells to the failed memory cells, the BIST computing unit having a register for storing addresses of the word lines and the bit lines of the failed memory cells, the BIST computing unit having a counter and, for each of the addresses, the counter increments a number relating to the failed memory cells as a hit value up to an upper limit, a corresponding one of the word lines or the bit lines being replaced in an event of the upper limit being exceeded (See Figure 6 and Summary of the Invention).

Regarding Claims 2, 4, 5, 18, 19, Pochmuller discloses in a test, the individual memory cell arrays are checked by driving their word lines and bit lines in order to determine defective memory cells, word lines and bit lines, where the results of the test

are stored in a register 12. A built-in-self-test (BIST) computing unit 14 with a counter unit 15 for counting the hit values up to an upper limit then evaluates the results of the tests. The results finally being stored in the registers 12, after the conclusion of the tests and determines those redundant memory cells, bit lines and word lines which, as the spare memory cells, spare bit lines and spare word lines from the memory cell array 10, are intended to replace the defective memory cells, bit lines and word lines in the memory cell arrays (1, 2, . . , n). The replacement of the memory cells, the bit lines and the word lines is effected, for example, via corresponding bus lines 11, which connect the individual memory cell arrays to one another.

Regarding Claims 6-8, 10-14, 16, Pochmuller discloses semiconductor memory configuration, Figure 6, containing memory cell arrays (1, 2, . , n), constructed as shown in Figure 1. In this case, it is possible to provide the redundant bit lines and the word lines with the corresponding memory cells in each of the memory cell arrays (1, 2, . , n). Likewise, however, it is also possible to accommodate the redundant bit lines and the word lines with the corresponding memory cells in a separate memory cell array 10, which is placed proximate to the BIST computing unit 14.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

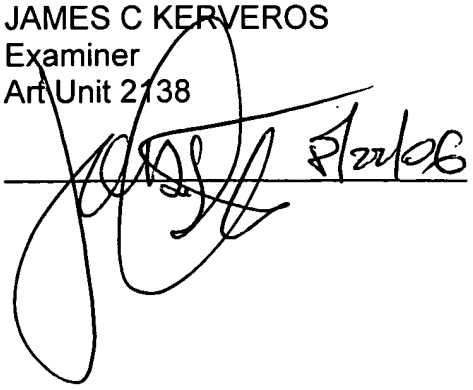
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Examiner
Art Unit 2138



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Date: August 22, 2006
Office Action: Final Rejection